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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,874	01/02/2001	Kazuhisa Fujimoto	501.39293X00	8035

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EXAMINER
MCLEAN MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	12

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,874	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-31,36-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16,18-30,36-39,41 and 42* is/are rejected.

7)☒ Claim(s) *6,7 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on April 2, 2003.

Oath/Declaration

2. Receipt is acknowledged of papers filed under 35 U.S.C. 119 (a)-(d) based on an application filed in Japan on May 18, 1998. Applicant has not complied with the requirements of 37 CFR 1.63(c), since the oath, declaration or application data sheet does not acknowledge the filing of any foreign application. A new oath, declaration or application data sheet is required in the body of which the present application should be identified by application number and filing date.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 22-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 22 recites the limitation "the memory unit" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 8-16, 18-30 and 38-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimoto et al. (USPN: 6,477,619).

Regarding claims 1 and 8, Fujimoto discloses a disk array controller comprising a channel interface package in which at least a channel interface unit with a host computer and access path interface are packaged (Figure 14, Reference 311 within Reference 201); a disk interface package in which at least a disk interface with a disk drive and an access path interface unit are packaged (Figure 15, Reference 312 within Reference 202); and a memory package in which a memory unit for storing control data for the disk drive and an access path interface unit are packaged (Figure 15, Reference 330 within Reference 202; C 16, L 50-51), wherein connections are made between the access path interface unit in the channel interface package and the access path interface unit in the memory package and between the access path interface unit in the disk interface package and the access path interface unit in the memory package by cables (Figure 15, References 231-232).

Regarding claims 2 and 9, Fujimoto discloses the disk array controller comprising plural memory packages, wherein connections are made between the access path interface unit in the channel

interface package an the access path interface unit in each of the plural memory packages by cables (Figure 14-15- each rack contains plural memory packages [330]).

Regarding claims 3 and 10, Fujimoto discloses the plural memory packages interconnected by cables (the memory packages in Reference 201 are interconnected to the memory packages in Reference 202 via cables).

Regarding claims 4 and 11, Fujimoto discloses that the memory units packaged in the plural memory packages store the same data (the same data stored in the memory packages is the same in that the data is received from the same sources).

Regarding claims 5 and 12, Fujimoto discloses that power is supplied from different power supplies to the plural memory packages (Figures 14 and 15 show different power supplies [350] supplied to the memory packages).

Regarding claims 13-16 and 18-21, Fujimoto discloses a disk array controller comprising a channel interface unit to be connected with a host computer (Figure 14, Reference 311 within Reference 201; Figure 1 shows the channel interface unit connected to a host computer); a disk interface unit to be connected with a disk drive (Figure 14, Reference 312 within Reference 201 – figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 15, Reference 330 within rack 202); an interface platter in which the channel interface unit and the disk interface are mounted (space inside of

rack 201 comprising a disk package 312 and a channel package 311); a memory platter in which the memory unit is mounted (space inside of rack 202 comprising a memory unit 330); a cable which couples the interface platter and the memory platter (Figure 15, References 231-232); a selector unit, coupled with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface unit and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system); wherein a path coupling the channel interface unit to the cable is printed in the interface platter (via References 222 and 340 within 201); wherein a path coupling the disk interface unit to the cable is printed on the interface platter (via References 222 and 340 within 201), and wherein a path coupling the memory unit to the cable is printed on the memory platter (via References 222 and 340 within 202).

Regarding claim 22, 27 and 38-39, Fujimoto discloses plural channel interface units each of which is coupled with a host computer (each of References 311 within References 201 and 202); plural disk interface units each of which is coupled with a disk drive (each of References 312 in Figure 14 within References 201 and 202); plural platters on each of which the channel interface unit, the disk interface unit and memory units (Reference 330 within References 201 and 202; C 16, L 50-51) are mounted (each space within racks 201 and 202, which each stores one of References 311, 312 and 330); a cable which couples the plural platters (platters in rack 201 are coupled to platters in rack 202 via cables 231-232); wherein a path coupling the channel interface unit to the cable is printed on each of the plural platters (each platter has a path coupling Reference 311 to References 340 and 222); wherein a path coupling the disk interface

unit to the cable is printed on each of the plural platters (each platter has a path coupling Reference 312 to References 340 and 222), and wherein a path coupling the memory unit to the cable is printed on each of the plural platters (each platter has a path coupling Reference 330 to References 340 and 222).

Regarding claims 24-26 and 28-29, Fujimoto discloses a selector unit, connected with the channel interface unit, the disk interface unit and the memory unit which are mounted on one of the plural platters, which selects requests from the channel interface and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system).

Regarding claim 30, Fujimoto discloses a channel interface unit to be connected with a host computer (Figure 14, Reference 311 within Reference 201; Figure 1 shows the channel interface unit connected to a host computer); a disk interface unit to be connected with a disk drive (Figure 14, Reference 312 within Reference 201 – figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 15, Reference 330 within rack 202); a first platter on which the channel interface unit is mounted (space within rack 201 which stores reference 311); a second platter on which the disk interface is mounted (space within rack 201 which stores reference 312); a third platter on which the memory unit is mounted (space within rack 202 which stores reference 330); a first cable which couples the first and third platters (Figure 15, Reference 231); a second cable which couples the second and third platters (Figure 15, Reference 232); wherein a path coupling the channel

interface unit to the first cable is printed on the first platter (the platter has a path coupling Reference 311 to References 340 and 222); wherein a path coupling the memory unit to the first and second cable is printed on the third plural platter (the platter has a path coupling Reference 312 to References 340 and 222 and References 231-232).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 36-37 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (USPN: 6,477,619).

Regarding claims 36 and 41, Fujimoto discloses a disk array controller comprising a channel interface unit to be connected with a host computer (Figure 14, Reference 311 within Reference 201; Figure 1 shows the channel interface unit connected to a host computer); a disk interface unit to be connected with a disk drive (Figure 14, Reference 312 within Reference 201 – figure 1 shows the disk interface unit connected to a disk drive); a memory interface unit for storing control data for the disk drive (Figure 15, Reference 330 within rack 202; C 16, L 50-51); an interface platter in which the channel interface unit and the disk interface are mounted (space inside of rack 201 comprising a disk package 312 and a channel package 311); a memory platter in which the memory unit is mounted (space inside of rack 202 comprising a memory unit 330); a cable which couples the interface platter and the memory platter (Figure 15, References 231-

232); a selector unit, coupled with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface unit and the disk interface unit (inherent, means is necessary in deciding which requests goes to what unit for proper functioning of the system); wherein a path coupling the channel interface unit to the cable is printed in the interface platter (via References 222 and 340 within 201); wherein a path coupling the disk interface unit to the cable is printed on the interface platter (via References 222 and 340 within 201), and wherein a path coupling the memory unit to the cable is printed on the memory platter (via References 222 and 340 within 202). Fujimoto does not explicitly disclose that the interface platter is perpendicular to the memory platter. However, it is known in the art that the lay out process for elements are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the interface platter perpendicular to the memory platter in Fujimoto's system to obtain specific design goals.

Regarding claims 37 and 42, Fujimoto discloses plural channel interface units each of which is coupled with a host computer (each of References 311 within References 201 and 202); plural disk interface units each of which is coupled with a disk drive (each of References 312 in Figure 14 within References 201 and 202); plural interface platters on each of which the channel interface unit and the disk interface unit are mounted (each space within racks 201 and 202, wherein each space stores one of References 311 and 312); a memory unit for storing control data for the disk drive (Reference 330 within rack 202; C 16, L 50-51); a memory platter in which the memory unit is mounted (space inside of rack 202 comprising memory unit 330); plural cables each of which couples each of the plural interface platters and the memory platter

(Figure 15, References 231-232); wherein a path coupling the channel interface unit to the cable is printed on each of the plural interface platters (each platter has a path coupling Reference 311 to References 340 and 222); wherein a path coupling the disk interface unit to the cable is printed on each of the plural interface platters (each platter has a path coupling Reference 312 to References 340 and 222), and wherein a path coupling the memory unit to the cable is printed on each of the plural memory platters (the platter has a path coupling Reference 330 to References 340 and 222). Fujimoto does not disclose the memory platter located between the plural interface platters. However, it is known in the art that the lay out process for elements are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the memory platter between the plural interface platters in Fujimoto's system to obtain specific design goals.

Allowable Subject Matter

9. Claims 6-7 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

June 15, 2003